1. (previously presented) A semiconductor wafer having an outer peripheral face containing a notch having an inner wall face extending inwardly and away from the outer peripheral face of the semiconductor wafer towards a center of the semiconductor wafer, wherein markings made from dot marks respectively having a maximum length of 1 to 13 μm are formed on the inner wall face.

2. (previously presented) The semiconductor wafer according to Claim 1, wherein upper and lower edge line portions of the inner wall face of the notch are respectively chamfered to thereby constitute upper and lower inclined faces and the dot marks are formed on the inclined faces.

3. (previously presented) The semiconductor wafer according to Claim 2, wherein an angle of an inclination of at least one inclined face relative to the surface of the semiconductor wafer is equal to or smaller than 30 degrees.

4. (previously presented) The semiconductor wafer according to Claim 2, wherein a surface roughness of at least one inclined face is equal to or smaller than 1 μm.

5. (previously presented) The semiconductor wafer according to Claim 2, wherein the dot marks are formed on either one of the upper and lower inclined faces.

6. (previously presented) The semiconductor wafer according to Claim 5, wherein an angle of an inclination of the inclined face relative to the surface of the semiconductor wafer is equal to or smaller than 30 degrees.

7. (previously presented) The semiconductor wafer according to Claim 5, wherein a surface roughness of the inclined face is equal to or smaller than 1 μm.

8. (previously presented) The semiconductor wafer according to Claim 1, wherein the dot marks are formed by irradiating a laser beam.

9. (previously presented) The semiconductor wafer according to Claim 1, wherein the dot marks have a height in the range of 0.005 to 5 μm.

10. (previously presented) The semiconductor wafer according to claim 1, wherein the markings include alphanumeric characters.

11. (previously presented) The semiconductor wafer according to claim 10, wherein a single font of the alphanumeric characters are arranged in a pattern of 5 dot marks by 9 dot marks.

12. (previously presented) The semiconductor wafer according to claim 1, wherein the markings are arranged on the inner surface of the notch prior to fabrication steps of a slicing step, and before mirror face fabrication step and chemical polishing step.

13. (previously presented) The semiconductor wafer according to claim 1, wherein the markings contain all the history information concerning fabrication steps for fabricating the semiconductor wafer.

14. (previously presented) A semiconductor wafer comprising a marked semiconductor wafer made from a semiconductor wafer that was subjected to at least one fabrication step that is visibly discernible on the marked semiconductor wafer;

the marked semiconductor wafer having an outer peripheral face containing a notch, the notch extending inwardly and away from the outer peripheral face of the semiconductor and towards a center of the

semiconductor, the notch having an inner wall face separated from and arranged inside the outer peripheral face of the marked semiconductor; the inner wall face of the notch containing markings, and the markings being dot marks having a maximum length of 1 to 13 μm.

15. (previously presented) A semiconductor wafer having a peripheral surface that was treated with processing steps, so that the peripheral surface contains visibly discernible structure resulting from the processing steps; and

the inner surface of the semiconductor wafer including a notch, the notch extending inwardly and away from the peripheral surface of the semiconductor and towards a center of the semiconductor, the notch having an inner wall face separated from and arranged inside the peripheral surface of the semiconductor; the inner wall face of the notch containing markings, and the markings being dot marks having a maximum length of 1 to 13 μm.

16. (new) The semiconductor wafer according to claim 1, wherein the notch has a shape so that a secluded portion of the inner wall face will not contact a member inserted into the notch for orienting the semiconductor wafer, and the markings are formed on the secluded portion of the inner wall face.

17. (new) The semiconductor wafer according to claim 14, wherein the notch has a shape so that a secluded portion of the inner wall face will not contact a member inserted into the notch for orienting the semiconductor wafer, and the markings are formed on the secluded portion of the inner wall face.

18. (new) The semiconductor wafer according to claim 15, wherein the notch has a shape so that a secluded portion of the inner wall face will not contact a member inserted into the notch for orienting the semiconductor wafer, and the markings are formed on the secluded portion of the inner wall face.